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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,490	08/29/2001	Tatsuo Furukawa	862.C2340	4851

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EXAMINER	
DIVINE, LUCAS	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,490	FURUKAWA, TATSUO	
	Examiner	Art Unit	
	Lucas Divine	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-14* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 1 – 14 are pending.

2. Applicant submitted a request to review an enclosed 1449. No such 1449 was found, and thus none is included in this action.

3. Claim objection and title objection withdrawn.

Response to Arguments

4. Applicant's arguments filed 8/31/05 have been fully considered but they are not persuasive.

With respect to applicant's arguments on page 8 that nothing in Corrigan teaches or suggests the new limitation.

In reply, Corrigan teaches a voltage generation circuit for generating the voltage by using a voltage for driving said printing element (Fig. 1A and col. 31 lines 16-17, wherein the voltage from the power supply 114 to 120 is used in all the circuits of the driver head, and thus includes the temperature sensor which includes the analog circuit) for driving said analog circuit is arranged on said element substrate (voltage generators 2942 and 2944 drive the components of temperature sensor 2915 [Fig. 29], col. 31 lines 64-65, col. 33 lines 1-20, col. 8 lines 59-60, wherein the sensors are on the driver head, thus the substrate [Fig. 6 also shows sensors 623 located on substrate]).

Thus, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3, 7, 8, 9, 10, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Corrigan, III et al. (US 6575548) hereafter as Corrigan.

Regarding claim 1, Corrigan teaches a **printhead** (126 Figs. 1A & 1B) **comprising an element substrate** (col. 2 line 1, Fig. 4, substrate 410; col. 7 lines 6 and 19) **having a printing element** (Fig. 1A, 120) **digital circuit and analog circuit** (col. 9 line 57),

said digital circuit including for selectively driving said printing element in accordance with input print data (Figs. 15, 17, 18, 19, 20, 21 and 23 are all digital circuits included in the driving of the printing element, more digital circuits are taught by Corrigan in other figures and in the description as well), **and**

said analog circuit including detection means for obtaining information (temperature sensor 2915, Fig. 29, col. 9 lines 52-53, measures information for keeping the printhead at appropriate temperatures),

wherein a value of a voltage for driving said digital circuit (col. 11 lines 19-21, wherein the logic circuitry with transistors can be at either VDD [5V] or VCC [12V]) **is**

different from a value of a voltage for driving said analog circuit (col. 33 lines 5-10 and 15-17 teach driving voltages for the temperature sensor at 5.12V and 2.7V)**, and**

a voltage generation circuit for generating the voltage by using a voltage for driving said printing element (Fig. 1A and col. 31 lines 16-17, wherein the voltage from the power supply 114 to 120 is used in all the circuits of the driver head, and thus includes the temperature sensor which includes the analog circuit) **for driving said analog circuit is arranged on said element substrate** (voltage generators 2942 and 2944 drive the components of temperature sensor 2915 [Fig. 29], col. 31 lines 64-65, col. 33 lines 1-20, col. 8 lines 59-60, wherein the sensors are on the driver head, thus the substrate [Fig. 6 also shows sensors 623 located on substrate])**.**

Regarding claim 3, which depends from claim 1, Corrigan teaches **voltage generation circuit generates the voltage for driving said analog circuit from a voltage for driving said printing element** (Fig. 1B teaches the power supply 114 powering the data processor and printer driver head 120, since this is the only power supply going to the print head, the varying voltages of the generators must be derived from the overall power supply driving the print head)**.**

Regarding claim 7, which depends from claim 1, Corrigan teaches **analog circuit comprises means for detecting an external temperature of said element substrate or means for monitoring a heater resistance value** (analog circuit is temperature sensor, col. 32 lines 46-50)**.**

Regarding claim 8, which depends from claim 1, Corrigan teaches **printhead is an inkjet printhead which ejects ink to print** (col. 1 line 12, col. 4 lines 10-11)**.**

Regarding claim 9, which depends from claim 8, Corrigan teaches **printing element comprises an electrothermal transducer for generating thermal energy to be applied to the ink so as to eject the ink using the thermal energy** (ink ejection element 416; col. 7 lines 20-22, wherein the ink ejection element acts as a heater [thermal transducer] to eject ink).

Regarding claim 10, which depends from claim 9, Corrigan teaches **detection means detects a temperature of said element substrate** (temperature sensor; col. 31 lines 16-17).

Regarding claim 13, Corrigan teaches that the printhead elements discussed in the rejection to printhead claim 1 are located inside printing apparatus (100 Fig. 1, 200 Fig. 2). Thus Corrigan teaches all of the structural elements of apparatus claim 13, and claim 13 is rejected for the same reasons as stated above in the rejection of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corrigan as applied to claim 1 above, and further in view of Deguchi et al. (US 5121135) hereafter as Deguchi.

Regarding claim 2, which depends from claim 1, Corrigan does not specifically teach **a capacitor arranged outside said element substrate and having one terminal connected to the voltage for driving said analog circuit and the other terminal grounded.**

Deguchi teaches a similar system including a thermal printing head with a thermister 105 (Fig. 11), the system including **a capacitor arranged outside said element substrate** (Fig. 11, capacitor and ground to the left of driving voltage Vin, also capacitor C1 is connected to ground; col. 5 lines 1-3) **and having one terminal connected to the voltage for driving said analog circuit** (the circuit that Vin is driving in Fig. 11 includes the thermister Rth) **and the other terminal grounded** (grounded at the lower left and below Ro).

It would have been obvious to one of ordinary skill in the art to have a capacitor attached to a voltage signal for a computing system as taught in Deguchi in order to prevent system failures of voltage dropping suddenly. The capacitor would slowly release the voltage when a system shutoff occurs, thus protecting the analog parts of the circuit from being blown out or otherwise damaged.

Regarding claim 14, which depends from claim 1, the same arguments of obviousness for capacitors used in claim 2 apply to the output of voltage from the voltage generation circuit, see C3 of Fig. 11 of Deguchi for the limitation to be met of connecting the output voltage to ground via a capacitor.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corrigan as applied to claim 1 above, and further in view of Yoshikawa et al. (US 5163063) hereafter as Yoshikawa.

Regarding claim 4, which depends from claim 1, while Corrigan teaches the system to have voltage generation circuits, Corrigan does not teach the specifics of the circuitry in the voltage generation circuits.

Yoshikawa teaches **said voltage generation circuit comprises a dividing resistor and a transistor** (col. 5 lines 14-21).

It would have been obvious to one of ordinary skill in the art to construct a voltage generation circuit with a dividing resistor and transistor. The motivation for doing so would have been to take a voltage powering the 5.12 voltage generation circuit 2942 and divide the voltage to 2.7 for the other voltage generation circuit 2944 (Fig. 29). This would allow for the internal sensing unit to only have one power lead to it and still supply both voltages to the needed parts, thus reducing complexity and cost.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corrigan as applied to claim 1 above, and further in view of Bhaskar et al. (US 5635968) hereafter as Bhaskar.

Regarding claim 5, which depends from claim 1, while Corrigan teaches the system to have voltage generation circuits, Corrigan does not teach the specifics of the circuitry in the voltage generation circuits.

Bhaskar teaches a voltage generation circuit for controlling a printing section of a thermal printer including **a noninverting amplifier** (1807, Fig. 18, col. 14 lines 60-65, wherein the thermal sense resistor RT is connected to the noninverting amplifier [specifically line 64]).

It would have been obvious to one of ordinary skill in the art that the voltage generation circuits could include noninverting amplifiers as taught in Bhaskar. The motivation for doing so would have been to take a low input voltage and boost the voltage to a needed level, thus the varying voltages of Corrigan could be attained with relatively low amounts of circuitry.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corrigan as applied to claim 1 above, and further in view of Kanbayashi et al. (US 6070959) hereafter as Kanbayashi.

Regarding claim 6, which depends from claim 1, Corrigan further teaches **digital circuit comprises a shift register for temporarily storing the print data** (shift register 2005, Fig. 20, col. 22 line 7) but does not specifically teach **a latch for holding the data stored in said shift register**.

Kanbayashi teaches an inkjet printing system similar to that of Corrigan including shift registers 71 in Fig. 5 that sends data to a latch circuit 70 for storing the data in the shift registers.

It would have been obvious to one of ordinary skill in the art that the shift register of Corrigan could include latches as taught in Kanbayashi. The motivation for doing so would have been to have separate shift clock and latch signals so that the timing of ink output could be more closely controlled (see Fig. 5 of Kanbayashi), the outputting does not have to be at the same time as the shifting.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corrigan as applied to claim 1 above, and further in view of Baumgartner et al. (US 6177815) hereafter as Baumgartner.

Regarding claim 12, which depends from claim 1, while Corrigan teaches driving the analog circuit at 5V (col. 33 line 9), Corrigan does not specifically teach **driving said digital circuit at 3.3 V.**

Baumgartner teaches that it is advantageous to power digital computing systems at 3.3V (col. 1 lines 18-20).

It would have been obvious to one of ordinary skill in the art to power the digital printhead circuitry at 3.3V as taught in Baumgartner. The motivation for doing so would have been to provide a printer that consumes less power (Baumgartner col. 1 line 18) and to be compatible with industry because many parts in the industry were going in the direction of 3.3V.

Allowable Subject Matter

7. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucas Divine whose telephone number is 571-272-7432. The examiner can normally be reached on Monday - Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lucas Divine
Examiner
Art Unit 2624

ljd

KING Y. POON
PRIMARY EXAMINER